DHAN-T Module

DECT-ULE Platform

Datasheet

Version: 2.2

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1. Introduction

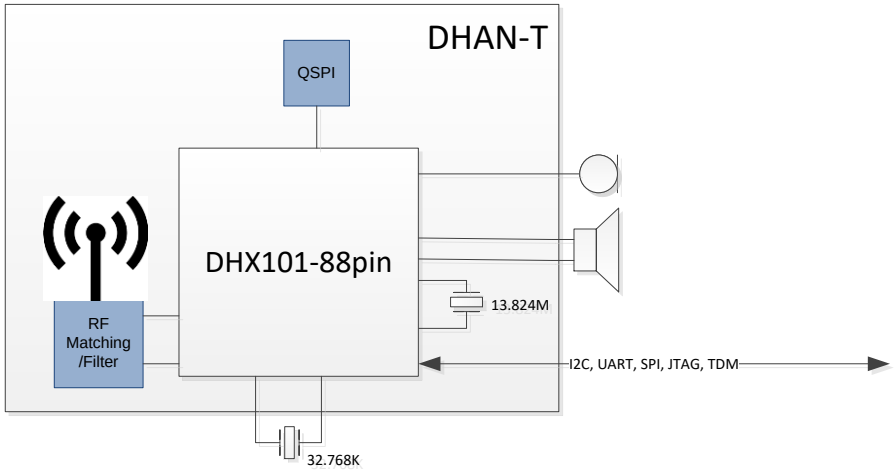
General Description

The DSPG DHAN-T module is based on the state-of-the-art DHX101 - a 4th generation DECT SOC. The DHAN-T module is well suited for all DECT and ULE Device applications. The DHAN-T SW stack includes standard DECT-ULE MAC-PHY connectivity as well as HAN-FUN (= the ULE Alliance Standard) functionality for Dual-Mode (data and audio) ULE. The Application SW written by the customer typically runs DHX101 within the DHAN-T. However the application Host can also run on external MCU which communicates with the DHAN-T via a UART interface.

Features

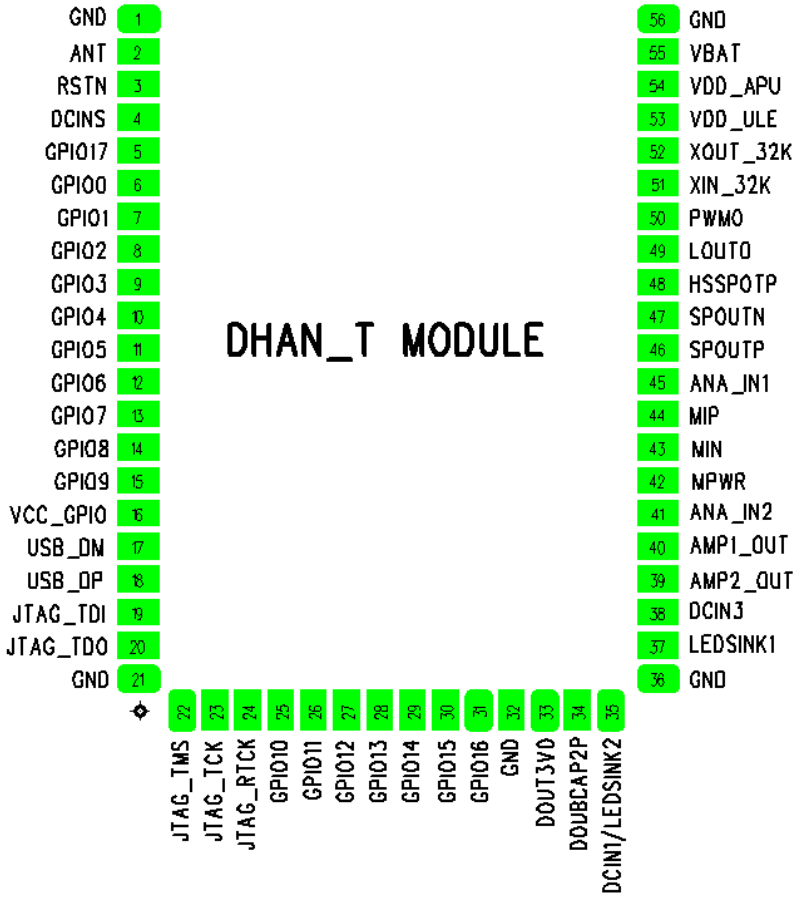
- Excellent radio performance, with over 119dB system gain
- A printed antenna is included in the module
- Radio covers all regional DECT bands. A simple re-configuration of the EEPROM is required
- Radio is fully compliant with ETSI DECT and ULE standards. Regulatory (EU, FCC) certification is pending
- Compact module with dimensions 27.2x16.9x3.3mm (including the RF shield height)
- Minimized external BOM
- Operating Temperature spanning -40ºC to 85ºC

Block Diagram



DHAN-T Module Block Diagram

2. Pinout and Signal Description



PIN NO.	NAME	DESCRIPTION/TYPE
1	GND	GND
2	ANT	Diversity Antenna. Leave unconnected
3	RSTN	For standalone operation, shunt this pin to GND with 100nF. For an application running on an external MCU, this pin should be connected to a Host MCU IO and used to reset the DHAN-T
4	DCINS	Leave as not connected (NC)
5	GPIO17	
6	SCL (GPIO0)	GPIO or I2C Clock. Open Drain, reset value is floating. Leave as not connected if not used
7	SDA (GPIO1)	GPIO or I2C Data. Open Drain, reset value is floating. Leave as not connected if not used
8	GPIO2	GPIO or TDM_TXD
9	GPI03	GPIO or TDM_RXD
10	GPIO4	GPIO or TDM_FSYNC
11	GPIO5	GPIO or TDM_FSYNC
12	GPIO6	GPIO or SPI Data In. Leave as not connected if not used
13	GPIO7	GPIO or SPI Data Out. Leave as not connected if not used
14	GPIO8	GPIO or SPI Clock
15	GPIO9	GPIO or UART Rx or SPI Chip Select
16	VCC_GPIO	Input. Sets the IO Logic level at the module interface at 1.8 or 3V
17	USB_DM	
18	USB_DP	
19	TDI	JTAG Data In. Should be connected to TP
20	TDO	JTAG Data Out. Should be connected to TP
21	GND	
22	TMS	JTAG Mode Select. Should be connected to TP
23	TCK	JTAG Clock. Should be connected to TP
24	RTCK	JTAG Reset. Should be connected to TP
25	GPIO10	GPIO or UART Rx or UART Tx
26	GPIO11	GPIO or UART Tx
27	GPIO12	GPIO
28	GPIO13	GPIO
29	GPIO14	GPIO
30	GPIO15	GPIO

PIN NO.	NAME	DESCRIPTION/TYPE
31	GPIO16	GPIO
32	GND	
33	DOUT3V0	3V (Doubler) Output. While DHAN-T is hibernating, this pin is either in tristate (default SW configuration) or pulled to GND. Can be used in conjunction with GPIO7&8 above to drive an LED or button during non-hibernation modes
34	DOUBCAP2P	Pull down with 1M resistor
35	LEDSINK2/DCIN1	ULE I/O. If not used, can be left NC
36	GND	GND
37	LEDSINK1/PWM	
38	DCIN3	ADC input used to monitor power supply input
39	AMP2_OUT	ULE I/O. Typically used (as input) to wake up the DHAN-T from hibernation
40	AMP1_OUT	ULE I/O. Typically used (as output) to indicate DHAN-T is active (logic high)
41	ANA2_IN	ULE I/O. During hibernate, Logic High should not be applied to this pin (it can result in leakage current). If not used, can be left NC
42	MPWR	Microphone Power
43	MIN	If not used, can be left as NC
44	MIP	If not used, can be left as NC
45	ANA_IN1	ULE I/O. If not used, can be left NC
46	SPOUTP	Speaker Output, Positive
47	SPOUTN	Speaker Output, Negative
48	HSSPOTP	Headset Speaker Out, Positive
49	LOUT	Headset Speaker Out, Negative
50	PWM0	Analog Output
51	XIN_32K	Connect to 32.768 XTAL
52	XOUT_32K	Connect to 32.768 XTAL
53	VDD_ULE	1.8V output. Active during hibernate. Can be used to power VCC_GPIO (Pin16)
54	VDD_APU	1.8V Test Point. Leave NC
55	VBAT	Power Supply Input. Connect to Battery or regulated 3V supply
56	GND	GND

3. Module Electrical Specifications

Unless otherwise noted, all specifications are for 25ºC.

Absolute Maximum Ratings

Minimum Voltage Applied to all pins: -0.3V
Maximum Voltage Applied to all pins: +4.6V
Storage Temperature Range: -45 to 90ºC

Note: Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

Table 3-1: Recommended Operating Conditions

RATING	CONDITIONS	MIN	TYP	MAX	UNIT
Operating ambient temperature		-40	+25	+85	°C
VBAT		1.95	3.0	3.6	V
All GPIOs Condition: VCC_GPIO is 3V	VIL VIH VOL VOH	 2.0 2.4		0.8 0.4	V
All GPIOs Condition: VCC_GPIO is 1.8V	VIL VIH VOL VOH	 1.17 1.35		0.63 0.45	V
RSTN	VIL VIH	 0.6*VBAT		0.3*VBAT	V
DCIN3		1.95	3.0	VBAT	V

Peak Currents and Hibernation Current

VBAT=3V

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
Tx Current	Band=EU @ 23dBm	400	480	mA
Tx Current	Band=US @ 21dBm	250	300	mA
Rx Current	Max Gain Setting	125	135	mA
Paging Current	1s response latency	90		µA
Hibernation Current		2		µA

Transmitter

VBAT=3V

Table 3-2: Tx Characteristics

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
NTP	Band=EU	21.5	23	24	dBm
NTP	Band=US	19	20	21	dBm
Harmonics	Band=EU & US		-40	-35	dBm
Transmission Mask	EN 301406 Paragraph 5.3.3		Comply		N/A
Frequency Offset	EN 301406 Paragraph 5.3.1	-50	8	+50	KHz
Frequency Drift	EN 301406 Paragraph 5.3.5	-15	0	+15	KHz/Slot
Emission Due Modulation	EN 301406 Paragraph 5.3.6.2 M±1 M±2 M±3 M>±3		 -20 -42 -47 -50	 -8 -30 -40 -44	dBm

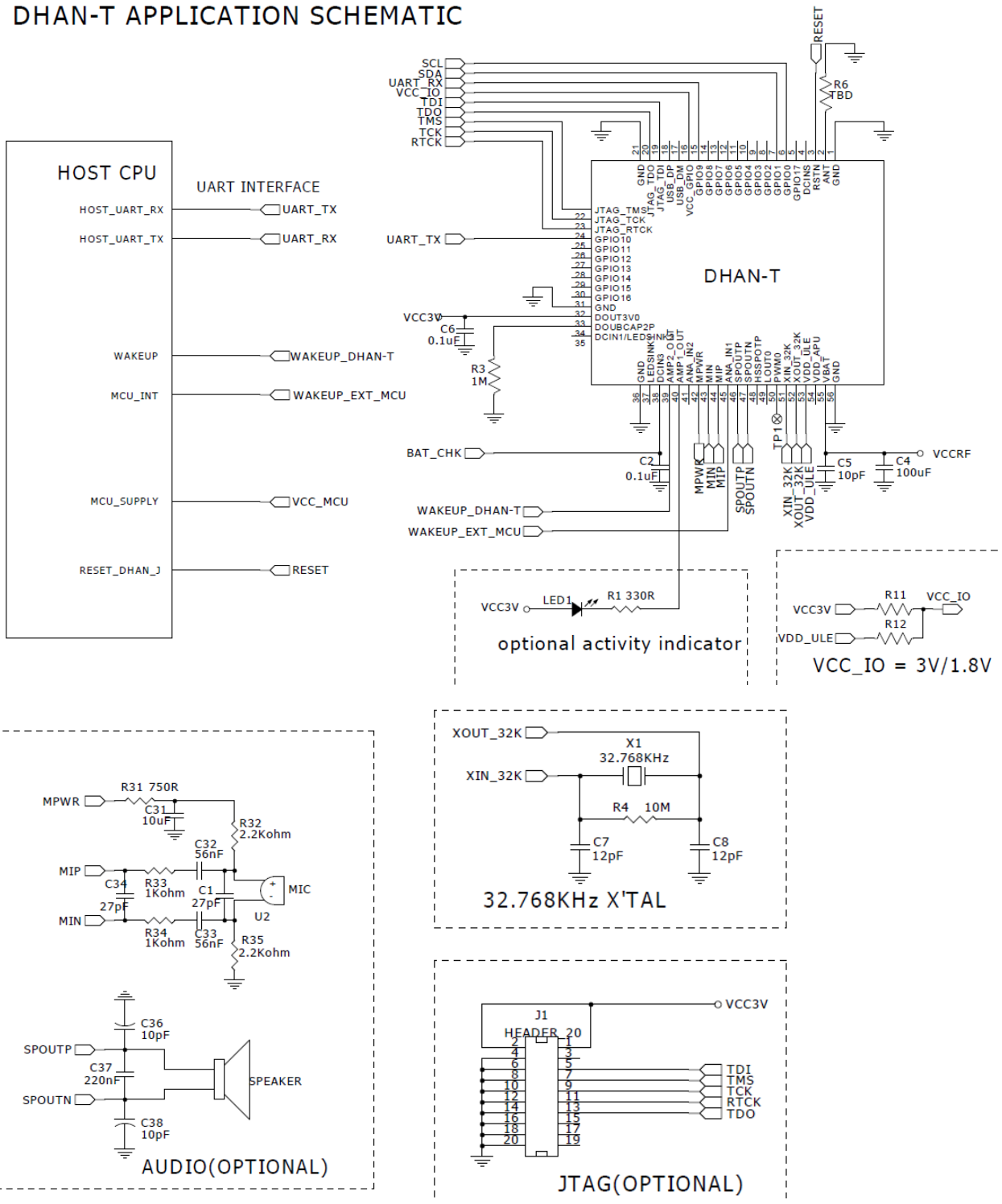
Receiver

VBAT=3V

Table 3-3: Rx Characteristics

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sensitivity, BER < 1000ppm	EU Band		-96	-93	dBm
Maximum input power	EU Band			15	dBm

4. ULE Application Reference Schematic



5. Interfacing the DHAN-T with an external MCU

RSTN Input

At power-up, the Application Host on the external MCU should hold this pin (Pin 3) at logic Low until it is ready to establish communication (via UART) with the DHAN-T. When ready, the App Host should apply a rising edge (and leave at Logic High) and wait for the “Hello” indication from the DHAN-T. If at some point later on the MCU cannot communicate with the DHAN-T, it should apply a low going pulse of >100uS to reset the DHX101 on the DHAN-T. Note that the RSTN pin is powered by the VBAT power domain. The minimum Logic High level is 0.6*VBAT.

UART, SPI Interfaces

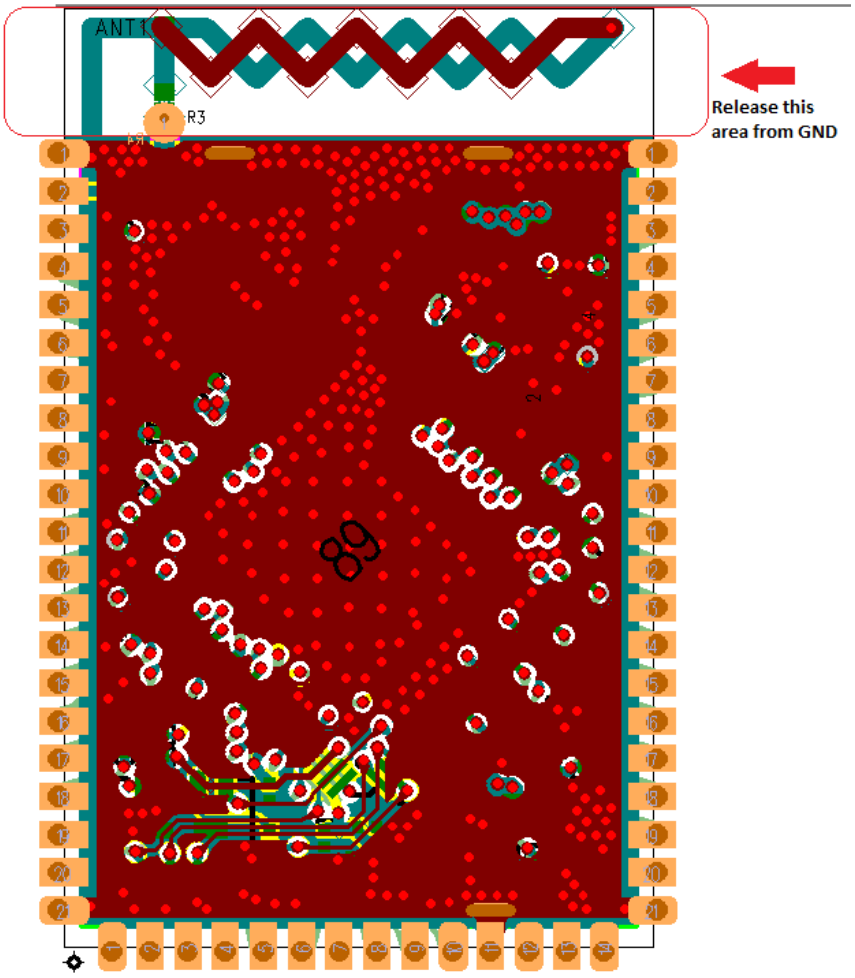
Applications requiring a UART I/F and an SPI interface (eg, SmartVoice ULE applications), will map the former to GPIOs 10 and 11 (Rx, Tx respectiveky) and the latter to GPIOs 6-9. Where only the UART I/F is required (as in the Reference Schematic provided above), UART Rx is assigned to GPIO9 and Tx to GPIO10.

6. Application PCB Design Recommendations

It is recommended that unused pads on the Application PCB not be left as isolated islands of copper but rather be anchored with via to inner layers of the PCB. It is also recommend that GND vias be applied liberally in the vicinity of GND pins 1, 21, 36 and 56.

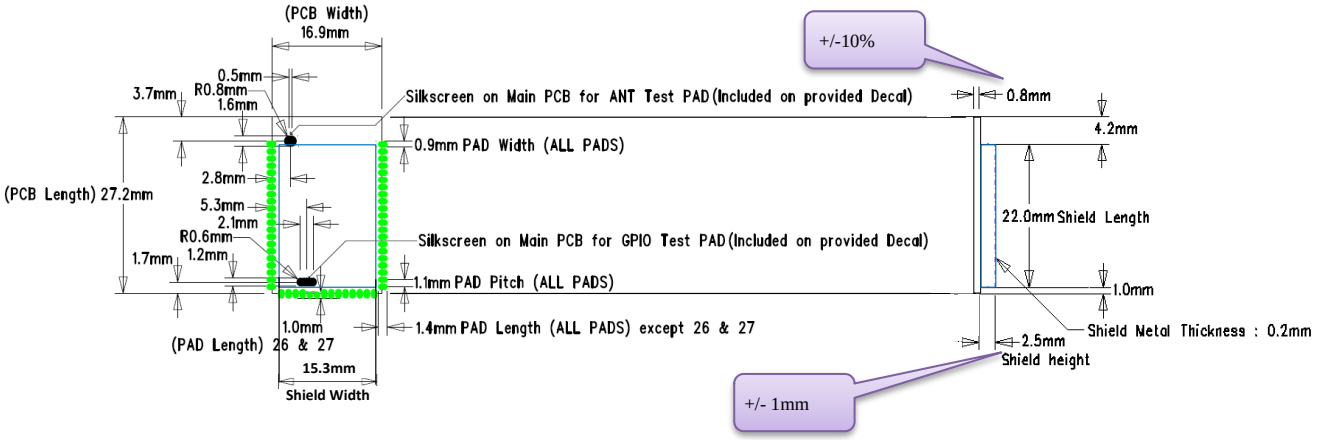
The following layout recommendations for embedding the DHAN-T on the Application Board:

1. Implement a solid ground under the DHAN-T module
2. Do not route signal traces under the module. Use the bottom layer for signal routing
3. Locate the antenna on the edge of the PCB
4. Release from GND on all layers under the DHAN-T antenna



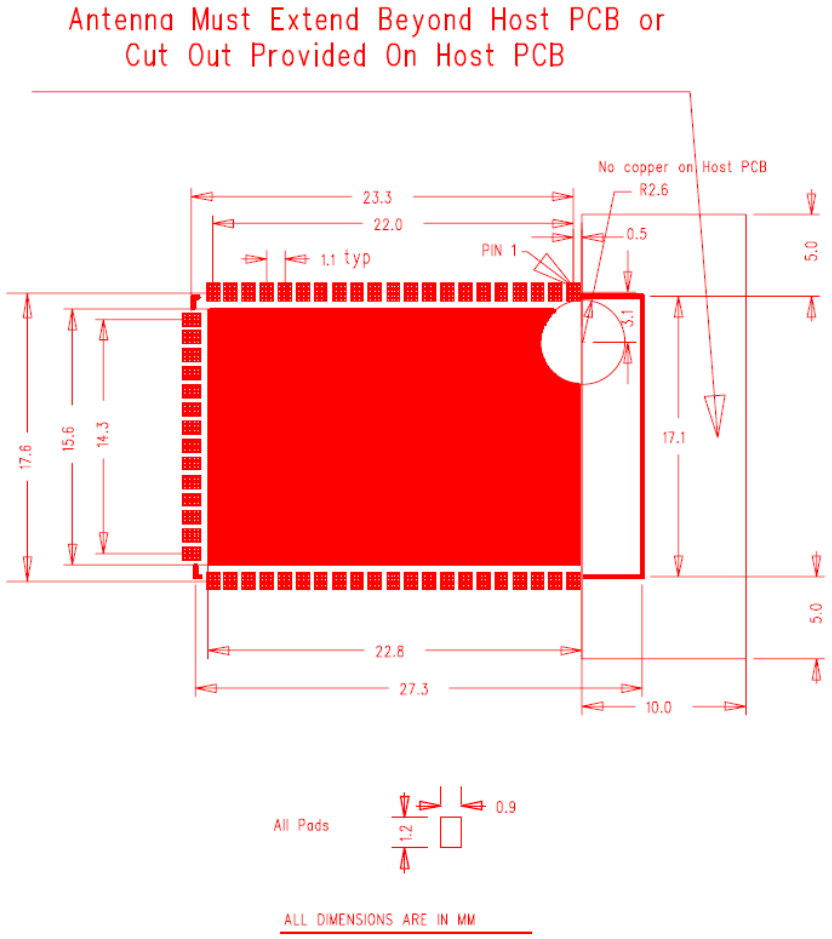
7. Assembly Information

Mechanical Drawing



PCB Footprint Detail

For an electronic version of this footprint, download from here



Pick & Place, Reflow

The DHAN-T module uses a flat shield cover to facilitate a fully automatic assembly process. For backing and reflow recommendations, use MSL 3 in the JEDEC/IPC standard J-STD-20b. The temperature classification (TC) for the module is 245° C.

8. Supplementary Information

Labeling (attached to the module shield)

1) Year
2) Week
3) 6-digit serial #
4) HW version
5) SW version

Handling Guidance

This module includes highly sensitive electronic circuity. Handling without proper ESD protection may damage the module permanently.

IPEI and EMC

Each DHAN-T Module is shipped to the customer with a unique IPEI – its DECT identity.

DHAN-T will ship with an “EMC” of 0xFEB. This is the DSP Group “generic” EMC. The EMC setting identifies a Device as belonging to a specific group of ULE Devices/Hubs that utilize some proprietary signaling.

In either case, the customer is free to re-program these parameters.

Ordering Information

Part #: DHX101MDMDFDA0AMI

Change Log

Table 8-1: List of Changes

REVISION	DATE	DESCRIPTION
1.1	June 4, 2018	Baseline release
1.2	August 8, 2018	Update PCB files
2.0	May 27, 2019	*Account for migration to DHX101, FW D (Part #, Block Diagram, paging idle current drain) *Clarifications to, VCC_IO RSTN (pinout description, drive by external MCU) *Clarifications to TDM, SPI mapping to GPIO *Added Reference Schematics
2.1	June 3, 2019	*Add detail PCB footprint drawing
2.2	April 16, 2020	*Clarify in Module Description that dimensions given are for the module itself, not the PCB footprint recommended for mounting the module *Replaced pinout diagram with more legible pin labels *Corrected JTAG TDO and TMS pin numbering in the tabulation. Now matches the diagram *Added labeling description *added tolerances to shield height and PCB thickness dimensions